Faculty Profile

Faculty Name: Dr.S.Govindarajulu
Department: ECE
Designation: Professor
Date of Joining the Institution: 06-05-2019

Faculty Description:

Dr.Salendra.Govindarajulu has a total of 23 years experience in academic & industry. Dr.Salendra.Govindarajulu is currently working as a Professor in the Dept. of Electronics & Communication Engg. at Dr.K.V.Subba Reddy Institute of Technology, Dupadu, Kurnool, Andhra Pradesh, India. Earlier he worked in RGMCET Nandyal for a period of 15 years, in GPREC Kurnool for a period of 2 years as a Professor of ECE. He also worked as Principal & Professor of ECE for a period of 2 years at VITS, Proddatur. He completed Ph.D in ECE(VLSI Design) in 2013, JNTUH Hyderabad, M. Tech in 2001, NIT, Calicut, Kerala, B. Tech in Electronics & Communication Engineering in 1999, JNTU Hyderabad. He worked as JTO, BSNL at Simla, Himachal Pradesh earlier. He presented more than 60 International/National Technical Papers in journals & conferences. He received a award certificate from NPTEL-SWAYAM (IIT Madras) for being recocgnized as NPTEL DISCIPLINE STAR in Electrical Engineering(ECE) on JAN-APR 2023. He participated in more than 55 International/National workshops & FDPs. He is a Life Member of ISTE, New Delhi, Member of IAENG & Member of ISRD. His Research interest includes Low Power VLSI CMOS design, Analog & Mixed VLSI, Wireless communications, etc. He supervised One Ph.D student and is currently guiding 5

Ph.D students. He supervised more than 30 M.Tech Theses. He published a book titled "Design of High Performance CMOS circuits using Domino Logic" by Scholar's Press, Deutschland, Germany with ISBN: 978-3-639-71281-0 in 2014. He worked as IQAC coordinator, NBA Convener, NAAC Convener etc. in various colleges.

Qualification:

Qualification	Institution	Year
B.Tech(ECE)	RGMCET, Nandyal, JNTU, Hyderabad.	1999
M.Tech (Power Electronics)	NIT Calicut (formerly REC Calicut), Kerala, University of Calicut.	2001
Ph.D. (ECE - VLSI Design)	JNTUH, Hyderabad.	2013

Experience:

Designation	Institution	From	To
Professor	DRKVSRIT, Kurnool	06-05-2019	Till Date
Professor	GPREC, Kurnool	01-05-2017	30-04-2019
Principal & Professor	VITS, Proddatur	06-11-2015	12-04-2017
Professor	RGMCET, Nandyal	31-10-2013	31-10-2015
Associate Professor	RGMCET, Nandyal	15-07-2007	31-10-2013
JTO (Junior Telecom Officer)	BSNL, Shimla dist, H.P State.	01-12-2006	09-07-2007
Associate Professor	RGMCET, Nandyal	01-07-2006	31-10-2006
Assistant Professor	RGMCET, Nandyal	18-12-2000	31-06-2006

Awards / Achievements:

- ✓ *A **JNTUA RATIFIED Professor***

NPTEL DISCIPLINE STAR AWARD in Electrical Engineering (ECE):

- ✓ Received a Certificate from NPTEL-SWAYAM (IIT Madras) for being recocgnized as NPTEL DISCIPLINE STAR in Electrical Engineering(ECE) on JAN-APR 2023. (Certified in courses of same discipline more than 50 weeks of learning, final score in each subject>55.)
- ✓ TEACHING AND LEARNING IN ENGINEERING (TALE)" (4 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Feb-March 2019 semester, IIT Madras.
- ✓ "MICROELECTRONICS:DEVICES TO CIRCUITS" (12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the JULY-OCTOBER 2019 semester, IIT Roorkee.
- ✓ "SWITCHING CIRCUITS AND LOGIC CIRCUITS" (12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the JULY-OCTOBER 2019 semester, IIT Kharagpur.
- ✓ "Digital Circuits" (12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2020 semester, IIT Khargapur.
- ✓ "Fundamentals of semiconductor devices" (12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2020 semester, IISc, Bangalore.
- ✓ "Integrated Circuits, MOSFETs, OP-Amps and their Applications" (12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2020 semester, IISc, Bangalore.
- ✓ "Antennas "(12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2020 semester, IIT Bombay.
- ✓ "Analog Circuits" (8 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2020 semester, IIT Bombay.
- ✓ "CMOS Digital VLSI Design" (8 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2020 semester, IIT Roorkee.
- ✓ "Transmission lines and Electromagnetic Waves" (12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2023 semester, IIT Madras.
- ✓ "RF and Microwave Networks" (12 Weeks) on the NPTEL-SWAYAM platform (swayam.gov.in), during the Jan-Apr 2023 semester, IIT Kharagpur.
- ✓ Successfully completed Electronic e-quiz on 02-06-2020 conducted by PDIT, Hosapet, Karnataka.

- ✓ Successfully passed in e-quiz –Engineer's role during pandemicss-on 03-06-2020 & 04-06-2020 conducted by AITS, Rajampet.

- ✓ Successfully completed online Faculty Programme onNBA on 05-11-2020 conducted by BVCOE, Navi Mumbai.
- ✓ Successfully completed e-quiz on MATLAB during 09-06-2020 to 13-06-2020 conducted by GPREC, Kurnool.
- ✓ Successfully completed online quiz on Review on VLSI Domain on 14-06-2020 conducted by GPREC, Kurnool.
- ✓ Successfully got Merit certificate in a one week online STTP conducted by AICTE on Machine learning on recent trends & applications phase-II from 24-05-2021 to 29-05-2021 conducted by SRIT,Anantapur.
- ✓ Successfully completed A three day online FDP on CMOS analog integrated circuits from 28-05-2020 to 30-05-2020conducted by SVREC, nandyal.
- ✓ Successful as Coordinatorr i/c, IQAC in securing NAAC A+ grade at GPREC in 2017-19.
- ✓ Successful as Professor i/c in securing 200+ recruitments in ECE at GPREC in 2018-19.
- ✓ Successful as Professor i/c in securing 20+ GATE ranks in ECE at GPREC in 2018-19
- ✓ Successful as Professor i/c in securing NBA for ECE at RGMCET, GPREC.
- ✓ 58 Research papers in reputed journals (8 SCOPUS & SCIE) and conferences
- ✓ Initiated and Developed NPTEL extension centre at VITS, Proddatur in 2015-17.

Responsibilities:

- ✓ Working as a faculty
  The following responsibilities are carried out as a faculty
  - Teaching regular Course Work
  - Mentoring the Students
  - Guiding the Junior Faculty
  - Continues research

Expertise / List of subjects handled:

- Antennas & Wave Propagation
- Electromagnetic waves & Transmission Lines
- Electronic Devices & Circuits
- VLSI Design
- Low Power Design

- Analog Communications
- Digital Electronics
- Linear Integrated Circuits & Applications
- Data Communications
- Computer Networks
- Network Theory
- FPGA A&A
- Satellite Communications
- Basic Electronics

Research Interest:

- Low Power VLSI Design
- Microelectronics
- Analog & Mixed signal design
- Wireless Communications

Publications:

Monograms Authored:

Title: "Design of High Performance CMOS circuits using Domino Logic"
ISBN: 978-3-639-71281-0 in 2014
Publishers: Scholar's Press, Deutschland, Germany

Patent:

Dr.S.Govindarajulu, Professor of ECE, et.al.

Title of the invention: "A SYSTEM FOR MANAGING POWER CONDUCTORS"

Patent application no. 201841042218; Date of filing of application: 09-11-2018; CBR Number: 31986; Country: India

Conferences:

International Conferences

1. S.Govindarajulu and Dr.T.J.C.Prasad "Consideration of performance Factors in CMOS Designs" ICED2008 International conference on Electronic design(IEEE) 1st-3rd December,2008 at Penang, Malaysia, **IEEE,Xplore-978-1-4244-2315-6/08.**
2. S.Govindarajulu and Dr.T.J.C.Prasad "Low-Power,High Performance Dual Threshold Voltage CMOS Domino Logic Circuits" International Conference on Recent Advancements in Electrical Sciences(ICRAES'10)8th and 9th jan'2010,Organized by Dept of EEE and ECE,KSR College of Engineering,Tiruchengode,Tamil Nadu,India,vol.III,No.1,pp109-118.
3. S.Govindarajulu and Dr.T.J.C.Prasad et.al "Temperature Variation Insensitive Energy – Efficient CMOS Circuits design in DSM Technology" Ist International Conference on Emerging Trenfs in Signal Processing and VLSI Design ,11th and 13th

June'2010,Organized by Dept of ECE,Guru Nanak Institutions (Guru Nanak Institutions Professional Activities),Hyderabad ,Andhra Pradesh,India,pp1179-1183.

4. S.Govindarajulu and Dr.T.J.C.Prasad et.al "Energy –efficient Low Voltage Swing Domino Logic Circuits in DSM Technology" Ist International Conference on Emerging Trenfs in Signal Processing and VLSI Design ,11th and 13th June'2010,Organized by Dept of ECE,Guru Nanak Institutions (Guru Nanak Institutions Professional Activities),Hyderabad ,Andhra Pradesh,India,pp946-951.
5. S.Govindarajulu et.al "Design of a high frequency hysteresis-controlled cmos buck converter for low power applications" in ICIEEE-2014 on 5th & 6th September 2014, pp.45, at Gurunanak Institutions, Hyderabad.
6. S.Govindarajulu et.al "Design methodologies for high performance vlsi adders in dsm technology" in ICIEEE-2014 on 5th & 6th September 2014, pp.302-308, at Gurunanak Institutions, Hyderabad.
7. S.Govindarajulu et.al "Design and implementation of high performance cmos latch designs in dsm technology" in ICIEEE-2014 on 5th & 6th September 2014, pp.267-273, at Gurunanak Institutions, Hyderabad.
8. S.Govindarajulu et.al "Novel fast and energy efficient carry skip adder in DSM technology" 2nd International Conference on Contemporary Engg. And Technology-ICCET-2018, PSCMR College of Engg. &Technology, Vijayawada,pp.51-52.
9. S.Govindarajulu et.al "High Performance Frequency Multiplier for DLL based Clock Generator in Nano Technology" 2nd International Conference on Contemporary Engg. And Technology-ICCET-2018, PSCMR College of Engg. &Technology, Vijayawada,pp.6-7.
10. S.Govindarajulu et.al "Design and Implementation of high performance CMOS latch designs in VDSM technology" ICSPECS-2019 11th and 12th of Jan-2019, pp-114, G.Pulla Reddy Engg. College, Kurnool.
11. S.Govindarajulu et.al "UWB-LNA with resistive feedback and shunt peaking using 0.18 µm." ICSPECS-2019 11th and 12th of Jan-2019, pp., G.Pulla Reddy Engg. College, Kurnool.
12. S.Govindarajulu et.al "Design of conditional boosting flipflop in nanometer technology" ICSCIE, Jawahar engg. College, Chennai, , pp-175,9th International conference.
13. S.Govindarajulu et al. "Design Optimization of Two Stage Operational Amplifiers using Chaotic Antlion Optimization" 4th IEEE-ICISC-2020, International conference on Inventive Systems & Control(IEEE), 8th-10th January,2020,pp.505-512, at JCT Institutions,Coimbatore, India, **IEEE,Xplore-978-1-7281-2813-9/20.**

National Conferences

1. S.Govindarajulu and Dr.T.J.C.Prasad "Runtime Leakage Power Reduction Techniques in DSM Technology:A Review" Second National Conference on Communication

technologies(NCCT'08),Dept of ECE,MEPCO SCHLENK Engineering college,SIVAKASI,TN-626006,INDIA on 14th -15th Mar,2008,pp280-285.

2. S.Govindarajulu and Dr.T.J.C.Prasad "Leakage Power Reduction Techniques In DSM Technology :A Review " Second National Conference on Communication Engineering NC-VCom 2008,Dept of ECE,SAINTGITS COLLEGE OF ENGINEERING, KottukulamHills.Pathamuttom,Kottayam, Kerala, INDIA on 14th -15th Mar,2008,pp311-313.
3. S.Govindarajulu and Dr.T.J.C.Prasad "Robust,Energy-Efficient and High Performance Domino Logic Circuits in DSM Technology " 2nd National Conference on Recent Trends in Electronics and Communication NCRTEC-2008,Dept of ECE, SJB Institute of Technology, BGS Health and Education City ,Uttarahalli Road, Kengeri, Bangalore -60 on 26th Mar,2008,pp1-7.
4. S.Govindarajulu and Dr.T.J.C.Prasad "Stand by and Runtime Leakage Power Reduction Techniques in DSM Technology" 2nd National Conference on Recent Trends in Electronics and Communication NCRTEC-2008,Dept of ECE, SJB Institute of Technology,BGS Health and Education City, Uttarahalli Road, Kengeri, Bangalore -60 on 26th Mar,2008,pp66-73.
5. S.Govindarajulu and et.al "Design of Energy-efficient and High performance VLSI adders", AICTE Sponsored NCSC-2014,March 22, 2014, pp.55-59.
6. S.Govindarajulu and et.al "Low leakage bit-line SRAM Design architectures", AICTE Sponsored NCSC-2014,March 22, 2014, pp.81-87.
7. S.Govindarajulu and et.al "Switching DC-DC converters with hybrid control schemes", AICTE Sponsored NCSC-2014,March 22, 2014, pp.116-120.

Journals:

International Journals Published:

1. S.Govindarajulu and Dr.T.J.C.Prasad "Low Power, Energy-efficient Domino Logic Circuits" , International Journal of Recent Trends in Engineering ,Vol 2,No.7,November 2009,Academy Press,pp30-33, ACEEE, Finland.**SEARCH Digital library,**SearchDl ID: 01.IJRTET.2.7.196
2. S.Govindarajulu and Dr.T.J.C.Prasad "Temperature Variation Insensitive Energy-Efficient CMOS Circuit Design in 65nm Technology" , International Journal of Engineering Science and Technology,Vol 2(6),2010,pp2140-2147,ISSN:0975-5462.**Open Access Indexed,ICV factor:3.14,**ISO 3297:2007,**Sci Rate indexed.**
3. S.Govindarajulu and Dr.T.J.C.Prasad "Energy-Efficient Reduced Swing Domino Logic Circuit in 65nm Technology",International Journal of Engineering Science and

Technology,Vol 2(6),2010,pp2248-2257,ISSN:0975-5462. **Open Access Indexed,ICV factor:3.14,**ISO 3297:2007

4. S.Govindarajulu and Dr.T.J.C.Prasad " Design of Low Power, High Speed, Dual Threshold Voltage CMOS Domino Logic Circuits with PVT Variations", International Journal of Electronic Engineering Research, Vol 2,Number 5,2010,pp619-629,ISSN:0975-6450.**Research India Publications journal.**
5. S.Govindarajulu and Dr.T.J.C.Prasad "High Performance VLSI Design Using Body Biasing in Domino Logic Circuits",International Journal on Computer Science and Engineering, Vol.2,No.05,2010,,pp1741-1745,ISSN:0975-3397.**Sci Rate indexed,Scirus indexed, Copernicus indexed.**
6. S.Govindarajulu and Dr.T.J.C.Prasad "Design of High Performance Dynamic CMOS Circuits in Deep Submicron Technology", International Journal of Engineering Science and Technology,Vol 2(7),2010,pp2903-2917,ISSN:0975-5462.**Open Access Indexed,ICV factor:3.14,**ISO 3297:2007,**Sci Rate indexed.**
7. S.Govindarajulu and Dr.T.J.C.Prasad "Design of energy-efficient Dual- V_tDomino Logic Circuits in 65 nm Technology", International Journal of Advances in Science and Technology,Vol 1 , No.3,2010,pp56-62,ISSN:2229-5216.**British &Europian library Indexed.**
8. S.Govindarajulu and Dr.T.J.C.Prasad "Robust,Energy-Efficient Reduced Swing Domino Logic Circuits", International Journal of Recent Trends in Engineering and Technology,Vol.3, No.4,May 2010,pp130-134, ACEEE, Finland.SearchDl ID: 01.IJRTET.3.4.73
9. S.Govindarajulu and Dr.T.J.C.Prasad "Performance Design metrics for CMOS Designs in DSM Technology", International Journal of Advances in Science and Technology ,Vol.2, No.3,March 2011,pp71-88, ISSN:2229-5216.**British &Europian library Indexed.**
10. S.Govindarajulu and Dr.T.J.C.Prasad "Design of High performance arithmetic and logic circuits in DSM Technology", International Journal of Engineering and Technology ,Vol.2, No.4, 2010,pp285-291, ISSN:0975-4024,**SCOPUS Indexed.**
11. S.Govindarajulu and Dr.T.J.C.Prasad et.al "Energy-efficient, domino VLSI circuits and their performance with PVT variations in DSM Technology", International Journal of Advanced Engineering Sciences and Technologies ,Vol.5, No.2, 2011,pp319-337, ISSN:2230-7818.**ICV:5.09,IEI Indexed.**
12. S.Govindarajulu and Dr.T.J.C.Prasad et.al "Energy-efficient, noise-immune CMOS domino VLSI circuits in VDSM Technology", International Journal of Advanced Computer Science and Applications,Vol.2, No.4, 2011, pp105-116, ISSN:2158-107X, The SAI Publishers, USA.**(SCI Expanded)IETInspec Direct indexed.Impact factor:1.34**
13. S.Govindarajulu and et.al "Design of Energy-efficient, High performance CMOS flip-flops in 65 & 120 nmTechnology", International Journal of Advances in Science and Technology ,Vol.2, No.3,March 2011,pp44-54, ISSN:2229-5216.

14. S.Govindarajulu and Dr.T.J.C.Prasad et.al "Multilayer AHB Bus matrix with self motivated arbitration scheme", International Journal of Advances in Science and Technology ,Vol.2, No.3,March 2011,pp9-17, ISSN:2229-5216.**British &Europian library Indexed.**

15. S.Govindarajulu and et.al "An efficient keeper technique for dynamic logic circuits", International Journal of Science and Advanced Technology ,Vol.2, No.5,May 2012,pp34-38, ISSN:2221-8386.**Sci Rate indexed,Copernicus Indexed.**

16. S.Govindarajulu and et.al "Novel keeper technique for Domino logic circuits in DSM Technology", International Journal of Latest Research in Science and Technology ,Vol.1, No.2,July-August, 2012,pp127-131, ISSN:2278-5299,**Copernicus Indexed,JournalIF:1.979.**

17. S.Govindarajulu and et.al "Image registration on satellite images", IOSR Journal of Electronics and communication engg.,Vol.3, Issue No.X, September-October, 2012,pp1-8, ISSN:2278-2834.**Impact Factor (African Quality Centre for Journals)AQCJ:1.586**

18. S.Govindarajulu and et.al "A Comparison of SIFT, PCA-SIFT and SURF", International journal of Innovative in Engg. & Research,Vol.6, Issue No.1, December, 2012,pp 53-60, ISSN:2319-5665.

19. S.Govindarajulu and et.al "Novel Low power and high speed array divider in 65 nm Technology", International Journal of Advances in Science and Technology ,Vol.6, No.6,March 2013,pp44-56, ISSN:2229-5216.**British &Europian library Indexed.**

20. S.Govindarajulu and et.al "Circuit optimization for Transmission gate Master Slave flip-flops", International Journal of Computers and Technology,Vol.11, No.3, October 2013,pp2387-2392, ISSN:2277-3061,**Impact factor:1.532.**

21. S.Govindarajulu and et.al "Performance of full adders with analyzation of logic and circuit implementation", International Journal of Electronics and Data Communication,Vol.3, No.4, December 2013,pp 47-54, ISSN:2278-5620.**Impact factor:0.637**

22. S.Govindarajulu and et.al "Design of Energy-efficient and High performance VLSI adders", International Journal of Engineering Research, Vol.3, Special Issue 2, March, 2014, pp.55-59, ISSN: 2319-6890)(online),2347-5013(print),**ISI (Thomson Reuters)Impact factor:0.732, Impact Factor(Research Bib) : 5.49**

23. S.Govindarajulu and et.al "Low leakage bit-line SRAM Design architectures", International Journal of Engineering Research, Vol.3, Special Issue 2, March, 2014, pp.81-87, ISSN: 2319-6890)(online),2347-5013(print),**ISI (Thomson Reuters)Impact factor:0.732, Impact Factor(Research Bib) : 5.49**

24. S.Govindarajulu and et.al "Switching DC-DC converters with hybrid control schemes", International Journal of Engineering Research, Vol.3, Special Issue 2, March, 2014, pp.116-120, ISSN: 2319-6890)(online),2347-5013(print),**ISI (Thomson Reuters)Impact factor:0.732, Impact Factor(Research Bib) : 5.49**

25. S.Govindarajulu and et.al "Design Of Novel Domino Circuits For High Performance And Energy Efficient VLSI Implementation " **International Journal of Applied**

Engineering Research (IJAER), Vol.10, No.17, 2015, pp.38219-38227, **(SCOPUS Indexed Journal)**

26. S.Govindarajulu and et.al "Design And Implementation Of Resistive Threshold Logic In DSM Technology " **International Journal of Applied Engineering Research (IJAER),** Vol.10, No.17, 2015, pp.38214-38218, **(SCOPUS Indexed Journal)**

27. S.Govindarajulu and et.al "Design of novel domino circuits for high performance and energy efficient VLSI design"Global Journal of Trends in Engineering**,**GJTE-Vol(2)-Issue(4) April 2015 ISSN: 2393-9923,pp.259-265.

28. S.Govindarajulu and et.al "MEMS Based Bio Applications: Advantages and Issues"International Journal of Emerging Technology &Engineering**,**IJETAE-Vol(6)-Issue(1) January 2016 ISSN: 2250-2459,pp.251-255.

29. S.Govindarajulu and et.al "Novel fast and energy efficient carry skip adder in DSM technology " Jour of Adv Research in Dynamical & Control Systems, Vol. 10, 05-Special Issue, 2018, pp.1024-1027, ISSN 1943-023X. **(SCOPUS Indexed Journal)**

30. S.Govindarajulu and et.al "High Performance Frequency Multiplier for DLL based Clock Generator in Nano Technology " International Journal of Pure and Applied Mathematics, Volume 118 No. 20, 2018, pp.4619-4625 ISSN: 1314-3395. **(SCOPUS Indexed Journal)**

31. S.Govindarajulu and et.al "Design and Implementation of high performance CMOS latch designs in VDSM technology." International Journal of Recent Technology and Engineering (IJRTE) : 2277 ISSN -3878, Volume-8, Issue-1S4, June 2019, pp-849-852. **(SCOPUS Indexed Journal)**

32. S.Govindarajulu and et.al "Design of conditional boosting flipflop in nanometer technology " Jour of Adv Research in Dynamical & Control Systems, Vol. 11, 03-Special Issue, 2019, pp-1609-1616, ISSN 1943-023X. **(SCOPUS Indexed Journal)**

33. S.Govindarajulu and et.al "UWB-LNA with resistive feedback and shunt peaking using 0.18 µm." Paper Presented in ICSPECS-2019**,** G.Pulla Reddy Engg. College , Kurnool, Publishing phase**.**

34. S.Govindarajulu and et.al "Multi Objective Optimization Of Two Stage Operational Amplifiers Using Antlion Optimization" International journal of scientific & technology research volume 8, issue 07, July 2019, pp.77-85, ISSN 2277-8616.

35. S.Govindarajulu and et.al "Optimization of Design Techniques by Reducing Power and Area of Two Stage CMOS Operational Amplifier Employing Salp Swarm Algorithm"

International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-8 June, 2019, pp.603-611.

36. S.Govindarajulu et.al "Optimization of Design Techniques by Reducing Power and Area of Two Stage CMOS Operational Amplifier Employing Salp Swarm Algorithm" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-8 Issue-8 June, 2019, pp.603-611. **(SCOPUS Indexed Journal)**

37. S. Govindarajulu et.al " Design Optimization of Two Stage Operational Amplifiers using Chaotic Antlion Optimization" (ICISC2020), IEEE-2020. (**IEEE International Xplore, SCOPUS**)

38. S. Govindarajulu et.al." Design Optimization of Power and Area of Two-Stage CMOS Operational Amplifier utilizing Chaos Grey Wolf Technique" IJACSA, Vol- 11, No:7 PP:261-270, July-2020. (**Web of Science (ESCI), SCOPUS & UGC recognized journal**)

39. Dr. S. Govindarajulu et.al." Implementation of Modified Vedic Multiplier using Quaternery Signed Digit Number System" Journal of Engineering Sciences, Vol- 13, Issue:12, 2022, **Page No :111-112 ISSN:0377-9254,** **DOI:10.15433.JES.2022.V13I12.43P.13**

40. Dr. S. Govindarajulu et.al." Implementation of Parallel TCAM with Soft-Error-Resilient SRAM for High-Scalability Search Applications" Journal of Engineering Sciences, Vol-13, Issue:12, 2022, **Page No :123-133, ISSN:0377-9254,** **DOI:10.15433.JES.2022.V13I12.43P.14**

National Journals

1. S.Govindarajulu, Dr.T.Jayachandra Prasad et.al. "Low Power, Reduced Dynamic Voltage Swing Domino Logic Circuits" Indian Journal of Computer Science and Engineering, Vol.1, No.2, 2010 pp.74-81, ISSN:0976-5166.

Faculty Development Programs and Workshops Attended:

1. Dr. S. Govindarajulu attended a workshop on "Human Values & Personality Development" in VITS, Proddatur conductd by NSS Unit on 12-01-2016.
2. Dr. S. Govindarajulu attended a workshop on "IBM Blue mix Enablement" in VITS, Proddatur on 28-12-2015.
3. Dr. S. Govindarajulu attended a workshop on "Analog Mixed Signal design using Tanner Tools" organized by Dept. of ECE in collaboration with ISTE in association with Ms.Shastra Micro Systems Pvt. Ltd., Hyderabad in RGMCET, Nandyal on 7th & 8th March, 2015.
4. Dr. S. Govindarajulu attended a One day workshop on "Formulation of Research & Development Initiatives for Engineering Faculty" conducted byESCI in association with FELIP, in RGMCET, Nandyal on 3rd November, 2014.

5. Dr. S. Govindarajulu attended a workshop on "Cloud Computing" organized by IT Dept. conducted by IEG in RGMCET, Nandyal on 17th & 18th October, 2014.
6. Dr. S. Govindarajulu attended a workshop on "Microwave Devices" organized by ECE Dept. conducted by Vajenthura Microwave Products, Chengalapattu in RGMCET, Nandyal on 06-08-2014.
7. Dr. S. Govindarajulu attended a workshop on "Loophole & Ethical Hacking Workshop" organized by AIESEC, IIT Kharagpur conducted by Kyrion Digital Securities (P) Ltd, at KGISL Institute of Technology, Coimbatore (Dept. of IT) on 21st & 22nd August, 2012.
8. Dr. S. Govindarajulu attended a **One Week** workshop on "VLSI, MW, DSP, P-Spice" organized by ECE Dept. in RGMCET, Nandyal from 10-05-2011 to 18-05-2011.
9. Dr. S. Govindarajulu attended a **One Week** workshop on "VLSI, MW, DSP, P-Spice" organized by ECE Dept. in RGMCET, Nandyal from 06-12-2010 to 15-12-2010.
10. Dr. S. Govindarajulu attended a National Level **One Week** workshop on "VLSI Electronic Systems" organized by ECE Dept. in RGMCET, Nandyal under TEQIP from 02-03-2009 to 07-03-2009.
11. Dr. S. Govindarajulu attended a Workshop for a **3 days** seminar on "High Speed Board Design" by M.S.Ramaiah School of Advanced Studies, Bangalore from 10-07-2008 to 12-07-2008.
12. Dr. S. Govindarajulu attended a National Level **One Week** workshop on "Full Custom & Semi Custom VLSI System Design" organized by ECE Dept. Under TEQIP in RGMCET, Nandyal from 27-02-2008 to 04-03-2008.
13. Dr. S. Govindarajulu attended a **One Week** workshop on "Technology & Design of VLSI and Embedded Systems" organized by ECE & ECM Depts. Under TEQIP in SNIST, Hyderabad from 27-31 August, 2007.
14. Dr. S. Govindarajulu attended a **One Week** workshop on "Microsoft Office" organized by CSE Dept. in RGMCET, Nandyal from 02-04-2007 to 09-04-2007.
15. Dr. S. Govindarajulu attended a **One Week** workshop on "Microsoft Office" organized by CSE Dept. in RGMCET, Nandyal from 02-04-2007 to 09-04-2007.
16. **One Week** National Workshop/FDP on Embedded System design & Applications from 14-05-18 to 19-05-18, at G.P.R.E.C(Autonomous), Kurnool.
17. **One Week** Workshop/FDP on Industrial Automation from 30-04-18 to 04-05-18, APSSDC-SIEMENS COE, JNTUA, Anantapuramu.
18. **Two Weeks** IIT Bombay FDP-101X-Sept-Oct.-2018-Foundation Program in ICT for education, Sept-Oct.-2018, National Conducted by **IIT Bombay**.
19. **Two Weeks** IIT Bombay FDP-201X-Nov-Dec-2018-Pedagogy for online blended Teaching, learning, Nov-Dec-2018, National Conducted by **IIT Bombay**.
20. A **12 week FDP** in NPTEL online course **TALE** Completed, National Conducted by **IIT Madras**.
21. **Two days** FDP for Heads of Departments of engineering colleges of Andhra Pradesh and Karnataka on the theme **Next Gen Technologies** - An Integrated Approach, from 22-05-2017 to 23-05-2017, at **TCS** Think Campus - Electronic City, Bangalore.

22. One day National Workshop/FDP on Networking Simulation using Qualnet Software on 14-09-2017, Dellsoft technologies Pvt. Ltd., New Delhi.
23. One day National Workshop/FDP on Circuit Simulation / PCB Design using Target3001! Software on 13-09-2018, Dellsoft technologies Pvt. Ltd., New Delhi.
24. Two days FDP on Outcome based education platform by IonCUDOS 7th & 8th of January 2019ICTIEE-2019, Malla Reddy Engg. College, IUCEE, Hyderabad.
25. Attended Two days FDP as a delegate for ICTIEE-2019, Malla Reddy Engg. College, IUCEE, Hyderabad, 7th & 8th of January 201

Online Workshops/FDPs attended (April 2020 to November 2020): 30

Invited Talks:

i) Delivered a presentation on Low power VLSI design using Microwind 3.1 tool at the workshop conducted by ECE Dept. in RGMCET, Nandyal, in 31-05-2011.

ii) Delivered a visiting Lecture in EMTL subject in Anurag College of Engg.,Hyderabad in 2011.

iii) Delivered a visiting Lecture in LICA subject in AVR&SVR Engg. College,Kurnool in 2012.

iv) Delivered a visiting Lecture in EMTL subject in AVR&SVR Engg. College,Kurnool in 2012.

v) Delivered a presentation on "Custom VLSI System Design using MICROWIND CAD BACKEND TOOLS" at SDP online workshop conducted by ECE Dept., Dr.KVSRIT on 23-06-2020 & 24-06-2020.

Memberships:

1. LIFE MEMBER in ISTE (Membership No.LM 34746)
2. LIFE MEMBER in IAENG (Membership No.113278)
3. LIFE time Fellow in ISRD (Membership No.F3140900459)

Google Scholar: h-index : 5

Elsevier Scopus: h-index : 2

Youtube Channel: https://www.youtube.com/channel/UCSaYFhzVQ2dDkepIo5F_VmQ

Blog: https://sgovindarajulu.blogspot.com/